**ANX7440/30/90/96 layout Checklist:**

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| **1** | **[Elective]**  Placement is important, please try to put ANX7440/30/90/96 to wide and open area. |  |
| **2** | **[Mandatory]** It’s important to have a complete VGND plane underneath, **and,**   * **VGND shall be out of the chip package. It is only for DC/DC circuits.** * VGND connect to GND at a single point which should be remote to ANX74xx and clean. * High speed traces should reference to GND and keep distance with VGND.   **EL: ok** | **Good Example:** |
| **3** | **[Mandatory]**  **Put 2 via when VGND fanout to inner layer**  **EL: please add one more via for VGND.** | **Example** |
| **4** | **[Mandatory]**  **Put all DC/DC components on VGND**  **EL:ok** | **Example Layout/schematic** |
| **5** | **[Mandatory]**  **DC/DC input decouple capacitor location, should be close to VIN pin**  **EL:ok** | **Good Example** |
| **6** | **[Mandatory]**  **1).** **Trace to VIN should be wide, shall fan-out as 8 mil wide trace. Increase width space available.**  **2). Fanout DC/DC VX output pin at 10mil width trace and widen it to inductor. Wider trace is better.**  **WL:1 ok. 2 ok.** |  |
| **7** | **[Mandatory]** Add a complete AVDD09 plane on layer VCC.  EL:ok | **Example layer**  E.g. Create a AVDD09 in layer 4, also see DVDD09, VDD18 |
| **8** | **[Mandatory]** Type C side AVDD09 pin has decouple capacitor (0.01uF) nearby. And, try to put all AVDD09 decouple capacitors near to pin(ANX7440).  **EL:ok** |  |
| **9** | **[Mandatory]**  **Length match rule: Differential pair P/N trace length match. (Ideally, length difference equal to zero)**   * **Length match to every section of the trace pair. E.g. pin to DC block capacitor, DC block capacitor to connector pin.**   **EL: please provide length table.** |  |
| **10** | **[Mandatory]**  **Length match rule: Inter-pair skew control, pair to pair length match with-in 500mil.**  **[Elective]**  **Length match rule: Inter-pair skew control, pair to pair length match with-in 50mil, for best margin without crowed routing, e.g. dense snake trace.**  **EL: please provide length table.** |  |
| **11** | **[Mandatory]**  **Spacing rule:**  **High-speed differential trace must keep 3xW (which is center to center distance) spacing to other net.**  **Snake trace should also keep 3xW distance to itself.**  **E.g. 3.5/3.5/3.5 trace should be around 3x7= 21 mil spacing to other net.**  **EL:ok** |  |
| **12** | **[Mandatory]**  **Spacing rule:**   * **XTAL and other noise component should keep distance from high speed lane as far as possible. Minim space is 3xW** * **The DC/DC inductor should be shielded component. If not, it should be 100mil away from the ANX7440** * **Keep high speed signal off DC/DC.100Mil clearance is best.**   **EL:** **Keep high speed signal off DC/DC.100Mil clearance is best.** |  |
| **13** | **[Mandatory]**  **Do not route power/high speed traces inside package area**  **EL: if possible, next time, remove SDA/SCL from inside package area.** | **Example:** |
| **14** | **[Mandatory]**  **Remove GND under USB/DP high speed decouple capacitors/resisters/ESDs, if their pad width is greater than 2xtrace width. Acceptable void could be as right.**  **EL: Remove GND under USB/DP high speed decouple capacitors/resisters/ESDs.** | **Example:** |
| **15** | **[Mandatory]**  **High speed differential trace impedance must keep along the trace. Reference plane must keep to GND.**  **DP/USB traces must center at differential 90 ohm** |  |
| **16** | **[Mandatory]**  **Max via number along a High-speed USB/DP trace are two.**  **EL:ok** |  |
| **17** | **[Mandatory]**  **SDA/SDC signal routing in pair**  **EL: please follow up next revision.** |  |
| **18** | **[Mandatory]**  **DP AUX signal routing in pair**  **EL: please modify in next revision** |  |
| **19** | **[Mandatory]**  **High speed trace keep distance to reference plane edge, it requires 4xW (which is center to center distance)**  **E.g. 3.5/3.5/3.5 trace should be around 4x7= 28 mil spacing to edge of reference plane**  **The minim spacing is 3xW**  **EL:ok** | Good example |
| **20** | **[Mandatory]**  **Stitching ground via is required for weak coupling differential vias that could not provide ideal return loop.**  EL: please follow up. |  |
| 21 | **[Mandatory]**  Power trace for VDD18, DVDD18 should be no less than 10mil  Power trace for VDD33 should be no less than 5mil  EL:ok |  |
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| 22 | **[Mandatory]**   * Stub on hi-speed trace should keep minim. E.g. If USB RX trace implement a pull-down resistor (Rb), usually 220K, then must not put a via on USB RX trace, the resistor must be very close to the trace, and ground point should be very close to resistor * USB RX traces shall not have any common-mode-choke, check schematic.   EL:ok |  |
| 23 | ESD devices should normally put close to the connector, avoid via.  **[Mandatory]**   * ESD devices should have good GND connection. ESD GND connect to ground immediately. * ESD device shall not leave any Stub on RX/TX traces.   EL: please add ESD components. |  |
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